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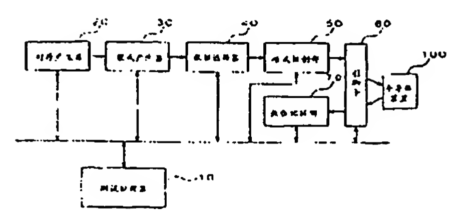
[54]发明名称 关键路径探索方法和探索系统

[57]摘要

本发明公开了使用实际的半导体装置能高速且可靠地检测出关键路径的关键路径探索方法和探索系统。将预定的数据输入到半导体装置中之后到输出与其对应的数据为止的工作时钟数目定为n,按顺序将该n个工作时钟的每一个的周期从失效周期变更为通过周期,进行关键路径的探索。



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权 利 要 求 书

1. 一种关键路径探索方法，其特征在于，包括:

第 1 步骤，检测出半导体装置是否正常工作的边界、即，检测出不正常工作的时钟信号的周期 T1 和进行正常工作的上述时钟的周期 T2；以及

第 2 步骤，将对上述半导体装置输入预定的数据之后到输出与其对应的数据为止的工作时钟数目定为 n，在将该 n 个工作时钟的一部分的周期设定为上述 T2 并将除此以外的周期设定为上述 T1 时，通过检验上述半导体装置是否正常工作来进行关键路径的探索。

2. 如权利要求 1 中所述的关键路径探索方法，其特征在于:

上述第 2 步骤包括:

确定关键路径的发生开始位置的第 3 步骤；以及

确定关键路径的发生区间的第 4 步骤。

3. 如权利要求 2 中所述的关键路径探索方法，其特征在于:

在上述第 3 步骤中，将从上述工作时钟的第（n-i）个到第 n 个为止的各周期设定为上述 T2、将除此以外的周期设定为上述 T1，检验上述半导体装置有无正常工作，将上述半导体装置进行正常工作的最大的（n-i）的值作为上述关键路径的发生开始位置来确定。

4. 如权利要求 2 中所述的关键路径探索方法，其特征在于:

在上述第 4 步骤中，将上述关键路径发生开始位置作为最前面的位置，将预定范围内包含的上述工作时钟的周期设定为上述 T2、将除此以外的周期设定为上述 T1，检验上述半导体装置有无正常工作，将上述半导体装置进行正常工作的最窄的上述预定范围作为上述关键路径发生区间来确定。

5. 一种关键路径探索系统，其特征在于，具备:

工作时钟发生装置，将对半导体装置输入预定的数据之后到输出与其对应的数据为止的工作时钟数目定为 n，发生半导体装置是否正常工作的边界、即，发生不进行正常工作的周期 T1 和进行正常工作的周期 T2 的各自的工作时钟；

试验数据输入装置，为了检验上述半导体装置的各自是否正常而对上述半导体装置输入预定的数据；

输出数据判定装置，在对应于用上述试验数据输入装置输入的预定

的数据从上述半导体装置输出数据时，判定该输出数据与所预期的数据是否一致；以及

探索控制装置，在从上述工作时钟发生装置输入到上述半导体装置的上述 n 个工作时钟中，将预定位置的工作时钟的周期设定为上述 T2 并将除此以外的周期设定为上述 T1，使上述半导体装置工作，根据上述输出数据判定装置对于与第 n 个工作时钟同步地从上述半导体装置输出的数据的判定结果，检验与周期为 T2 的工作时钟的位置对应的关键路径的有无。

6. 如权利要求 5 中所述的关键路径探索系统，其特征在于：

上述探索控制装置将从第 n 个上述工作时钟到第（n-i）个的上述工作时钟为止的各周期设定为上述 T2、将除此以外的周期设定为上述 T1，检验上述半导体装置有无正常工作，将上述半导体装置进行正常工作的最大的（n-i）的值作为关键路径的发生开始位置来确定。

7. 如权利要求 6 中所述的关键路径探索系统，其特征在于：

在上述探索控制装置将从上述工作时钟的第（n-i）个到第 n 个为止的各周期变更为上述 T2 并检验上述半导体装置有无正常工作时，使 i 的值逐渐增大。

8. 如权利要求 6 中所述的关键路径探索系统，其特征在于：

上述探索控制装置将上述关键路径发生开始位置作为最前面的位置，将预定范围内包含的上述工作时钟的周期设定为上述 T2、将除此以外的周期设定为上述 T1，检验上述半导体装置有无正常工作，将上述半导体装置进行正常工作的最窄的上述预定范围作为关键路径发生区间来确定。

9. 如权利要求 8 中所述的关键路径探索系统，其特征在于：

在上述探索控制装置将上述工作时钟的一部分周期变更为上述 T2 并检验上述半导体装置有无正常工作时，使上述预定范围逐渐增大。

10. 如权利要求 5 中所述的关键路径探索系统，其特征在于：

上述半导体装置具有与从外部输入的工作时钟同步地生成另外的内部时钟的 PLL 电路。

说　　明　　书

关键路径探索方法和探索系统

本发明涉及进行各种大规模集成电路（LSI）的关键路径（critical path）的确定的关键路径探索方法和探索系统。再有，在本说明书中，所谓「半导体装置」，是表示逻辑电路、存储电路、模拟电路、或将这些电路组合起来的半导体器件的整体的装置。

目前，集成在 LSI 中的晶体管的数目正在飞跃地增加，特别是以微处理器为代表的逻辑 LSI、存储器、模拟 LSI、系统 LSI 的电路的复杂度正在不断增加。在进行这样的以大规模且复杂、高速工作的 LSI 的不良分析并将其反馈到设计中去的情况下，频繁地进行找出 LSI 内的关键路径的操作。所谓该关键路径，指的是在 LSI 内的信号传送路径内制约整体的电路工作速度的特定的路径，在 LSI 设计中必须将这些路径的传播时间抑制在预定值以下。

迄今，LSI 内的关键路径的探索是利用基于设计数据的模拟来进行的。在构成 LSI 的各电路中，根据其设计数据，可利用模拟来算出通过从信号的输入到输出间的各种运算电路、存储电路等的传播时间。因而，利用计算可求出在输入预定的测试矢量（测试模式（pattern））时在 LSI 内部进行怎样的工作，关键路径的探索成为可能。

但是，在如上所述那样利用模拟求出 LSI 内的关键路径的现有方式中，存在下述等问题：

（1）编制进行验证全部逻辑信号的关键路径的模拟的程序是非常费时的；

（2）由于没有使实际的电路（半导体装置）工作，故有不能用负载的设定等的模拟来表现的情况，以及因难以表现故在其设定中非常费时的情况；

（3）由于进行庞大的数值数据处理，故在探索方面非常费时。

本发明的目的在于提供一种能使用实际的半导体装置高速且可靠地检测关键路径的关键路径探索方法和探索系统。

在一个优选的实施例中，在本发明的关键路径探索系统和该系统中使用的探索方法中，着眼于在缩短工作时钟的周期并达到周期 T1 而不进行正常工作时，能通过使对应于关键路径的位置的工作时钟的周期稍

许变长成为 T2 而使半导体装置正常工作，通过检验如果将输入数据之后到输出为止的n个工作时钟中的第某个工作时钟的周期从T1变更为T2则半导体装置是否正常工作来进行关键路径的探索。

具体地说，利用工作时钟发生装置将输入到半导体装置中的 n 个工作时钟的周期设定为 T1 或 T2，在对应于用试验数据输入装置输入的数据与上述的 n 个工作时钟同步地工作后，利用输出数据判定装置检验从半导体装置输出的数据的正确与否，在该输出数据正确时，即在半导体装置正常工作时，探索控制装置判断为在周期为 T2 的工作时钟的位置上存在关键路径，从而进行关键路径的探索处理。

这样，按照本发明，通过使半导体装置实际进行工作来进行关键路径的探索，与利用模拟来探索关键路径的情况相比，能高速且可靠地检测关键路径。此外，可进行负载设定等来使半导体装置工作，故可进行考虑了实际使用状态的探索处理。

此外，最初的目标是，利用上述的探索控制装置，从第 n 个工作时钟开始，将第（n－i）个区间的工作时钟的各周期设定为 T2、除此以外的周期设定为 T1，检验半导体装置有无正常工作，将进行正常工作的（n－i）的值确定为发生关键路径的开始位置。此外，第 2 个目标是，利用探索控制装置将发生关键路径的开始位置作为最前面的位置，将在预定范围内包含的工作时钟的周期设定为 T2、除此以外的周期设定为 T1，检验半导体装置有无正常工作，将进行正常工作的最窄的范围确定为发生关键路径的区间。这样，通过确定发生关键路径的开始位置和发生关键路径的区间，可正确地探索关键路径的发生位置，可容易地制定设计变更等的对策。

此外，本发明适用于具有与从外部输入的工作时钟同步而生成另外的内部时钟的 PLL 电路的半导体装置的关键路径的探索。在本发明的关键路径探索方式中，由于也能以半导体装置进行正常工作或不进行正常工作的边界附近的工作时钟周期 T1 和 T2 使半导体装置工作，故在 T1 和 T2 之间变更从外部输入的工作时钟的周期时，由内部的 PLL 电路生成的内部时钟容易跟随该工作时钟，因此改变上述的工作时钟的周期来进行关键路径的探索的本发明的探索方式的应用变得容易。

图 1 是示出本实施例的半导体试验装置的结构的图;

图 2 是说明利用本实施例的半导体试验装置进行的关键路径探索的

原理用的图；

图 3 是示出半导体装置的输入输出模式与工作时钟周期的关系的图；

图 4 是示出探索发生关键路径的开始地址的工作程序的图；

图 5 是示出发生开始地址与为了对其进行确认而设定的各地址的工作周期的关系的图；

图 6 是示出探索发生关键路径的区间的工作程序的图；

图 7 是示出发生区间与为了对其进行确认而设定的各地址的工作周期的关系的图；

图 8 是示出输入到在内部具有 PLL 电路的半导体装置中的外部时钟与内部时钟的关系的图；以及

图 9 是示出输入到在内部具有 PLL 电路的半导体装置中的外部时钟与内部时钟的关系的图。

应用了本发明的实施例的半导体试验装置的特征在于，将预定的模式数据输入到作为关键路径的探索对象的半导体装置中，同时通过将各测试周期的工作时钟周期设定为 pass（正常工作）和 fail（不良工作）的边界的值以使半导体装置工作来进行关键路径的探索。以下，一边参照附图，一边说明应用了本发明的一个实施例的半导体试验装置的详细情况。

图 1 是示出本实施例的半导体试验装置的结构的图。在该图中示出的半导体试验装置为了相对于作为关键路径的探索对象的半导体装置 100 而输入输出在探索工作方面所必须的各种信号，其结构包括：测试处理器 10、时序产生器 20、模式产生器 30、数据选择器 40、格式控制部 50、引脚卡（pin card）60 和数值比较部 70。

上述的测试处理器 10 利用操作（operating）系统（OS）来执行预定的测试程序，为了探索半导体装置 100 内的关键路径而对半导体试验装置的整体进行控制。时序产生器 20 设定探索工作方面所必须的基本周期，同时生成该已设定的基本周期内包含的各种定时沿（timing edge）。模式产生器 30 产生输入到包含半导体装置 100 的时钟端子的各端子的模式数据。数据选择器 40 使从模式产生器 30 输出的各种模式数据与输入该数据的半导体装置 100 的各端子相对应。格式控制部 50 根据由模式产生器 30 产生并由数据选择器 40 选择的模式数据和由时序产生器 20 生成的定时沿，进行对于半导体装置 100 的波形控制。

此外，引脚卡 60 用于作为与半导体装置 100 之间的物理的接口．例如，在引脚卡 60 中包括将预定模式波形施加到半导体装置 100 的对应的端子上的驱动器和进行在各端子上呈现的电压波形与预定的低电平电压和高电平电压的比较的比较器．数值比较部 70 相对于半导体装置 100 的各端子的输出数据，进行与由数据选择器 40 选择的各端子的每一个预期值数据的比较。

利用时序产生器 20 生成供给半导体装置 100 的时钟信号及其它的时序信号，利用模式产生器 30 生成输入到半导体装置 100 中的各种数据。此外，利用数值比较部 70 来判断输入到半导体装置 100 中并使其工作几个预定的测试周期之后的半导体装置 100 的输出数据是否正常．

上述的时序产生器 20 对应于工作时钟发生装置，模式产生器 30 和数据选择器 40 对应于试验数据输入装置，数值比较部 70 对应于输出数据判定装置，测试处理器 10 对应于探索控制装置．

本实施例的半导体试验装置具有这样的结构，其次，说明使用该装置进行半导体装置 100 内部的关键路径的探索的情况的详细的工作．

图 2A 和图 2B 是说明利用本实施例的半导体试验装置进行的关键路径探索的原理用的图．在图 2A、图 2B 中，地址（1）、（2）等对应于测试周期的数目、即，输入的工作时钟的个数．例如，地址（6）示出了输入测试模式并与第 6 个工作时钟同步地工作的位置（电路）．

如图 2A 中所示，将逐渐缩短工作时钟的周期从而输出模式成为不良的周期设为 T1．此时，如果能知道输出模式是否由于对应于某一个地址的电路不能正常地工作而成为不良，则可将该不良部位作为发生关键路径的部位来探索。

例如，如图 2A 中所示，在对应于地址（4）的位置上产生工作异常而输出模式成为不良的情况下，如图 2B 中所示，通过使对应于地址（4）的第 4 个工作时钟的周期变更为比 T1 稍长一些的 T2，可得到正常的输出模式。

这样，在将全部测试周期的工作周期设定为失效的 T1 的状态下，通过检验使对应于哪个地址的工作周期加长能达到正常工作，可找出发生关键路径的地址．在本实施例中，通过检测发生关键路径的开始地址和发生关键路径的区间两者来进行关键路径的探索处理。

图 3 是示出半导体装置 100 的输入输出模式与工作时钟的周期的关

系的图．例如，在对半导体装置 100 的输入引脚 1 输入预定的试验数据（在图 3 的地址（1）中为“0”）之后输入了 7 个工作时钟时，如果在输出引脚 1 上呈现对应于该试验数据的输出数据，则通过检验该第 7 个时钟的输出数据与预期值是否一致，可知道对应于打算检验的地址的电路的工作是否正常。

例如，在只将对应于图 2B 中示出的地址（4）的工作周期设为 T2、将除此以外的工作周期设为 T1 的情况下，将图 3 中示出的 t1～t3 和 t5～t7 的每一个设定为 T1、只将 t4 设定为 T2．这样，只将第 4 个工作时钟的周期设定为 T2，使半导体装置 100 工作 7 个时钟，检验在该工作后在输出引脚 1 上呈现的输出数据是否与预期值一致。

其次，将关键路径的探索工作分成发生关键路径的开始地址的探索工作和发生关键路径的区间的探索工作的情况来说明．例如，如图 3 中示出的那样，对输入引脚 1 输入试验数据之后使其工作 7 个时钟时，输出对应于输出引脚 1 的数据．此外，作为在对应于地址（4）～（6）的位置上存在关键路径的情况来进行说明。

图 4 是示出探索发生关键路径的开始地址的工作程序的图。首先，测试处理器 10 使供给半导体装置 100 的工作时钟的周期变化，寻找成为工作失效和通过的边界的工作周期（步骤 a1）。该工作周期的变更通过将指令送给时序产生器 20 来进行，在使用各自的周期的工作时钟时的半导体装置 100 是否正常工作的判断，是通过如图 3 中示出的那样将对应于全部地址的工作周期设定为某个值，并检验与第 7 个时钟同步地得到的输出引脚 1 的输出数据来进行的。通过这样做，检测出失效的工作时钟的周期 T1 和通过的工作时钟的周期 T2，即检测出上述的边界。

其次，测试处理器 10 将指令送给时序产生器 20，将全部地址的工作周期设定为失效周期 T1（步骤 a2）。将图 3 中示出的全部工作周期 t1～t7 设定为 T1。

通过这样做，在将全部工作周期设定为失效周期 T1 后，测试处理器 10 将发生关键路径的开始地址（以下，简单地称为「发生开始地址」）设定为半导体装置 100 失效的地址（以下，称为「失效地址」）（7）（步骤 a3），将该发生开始地址以后的各地址的工作周期设定为通过周期 T2（步骤 a4）。然后，对于半导体装置 100 进行预定的工作试验（步骤 a5），判定在输出引脚 1 上呈现的输出数据是否是正常值（与预期一

致的值）（步骤 a6）。

图 5A－图 5D 是示出发生开始地址与为了对其进行确认而设定的各地址的工作周期的关系的图．如图 5A 中所示，在上述的步骤 a3 中将发生开始地址设定为（7）的情况下，只将 n 个工作时钟内的第 n 个（由于在实施例中 n＝7，故是第 7 个）地址（7）的工作周期变更为 T2 来进行工作试验。

以这种方式进行实施的工作试验的结果，在输出引脚 1 上呈现的输出数据是与预期一致的正常的数据的情况下，将在该时刻设定的发生开始地址确定为关键路径的发生开始地址（步骤 a7），关键路径的发生开始地址的探索处理结束。

此外，工作试验的结果，在输出引脚 1 上呈现的输出数据不正常的情况下，测试处理器 10 下一步判断在该时刻设定的发生开始地址是否是最前面的地址（1）（步骤 a8）。由于最初在上述的步骤 a3 中将发生开始地址设定为失效地址（7），故判断为否定，测试处理器 10 在将发生开始地址向最前面方向进 1 并设定为地址（6）（步骤 a9）后，重复上述的步骤 a4 的工作周期的设定以后的处理．

如图 5B 中所示，在将发生开始地址进 1 设定为地址（6）的情况下，将该地址（6）以后、即地址（6）和（7）设定为通过周期 T2，实施工作试验。

此外，即使在将地址（6）和（7）设定为通过周期 T2 并实施工作试验、在输出引脚 1 上也不呈现正常的输出数据的情况下，如图 5C 中所示，在将发生开始地址再进 1 设定为地址（5）后，重复上述的步骤 a4 的工作周期的设定以后的处理．

通过这样做，将发生开始地址逐一向最前面一侧行进、将该发生开始地址以后的各地址的工作周期设定为通过周期 T2，通过每次都进行工作试验，重复该程序，直到在输出引脚 1 上呈现正常的输出数据．例如，如图 5D 中所示，在将发生开始地址设定为地址（4）、将地址（4）～（7）的工作周期设定为通过周期 T2 并实施工作试验时在输出引脚 1 上呈现正常的输出数据的情况下，如上述那样在步骤 a6（输出数据是否正常的判定处理）中判断为肯定，将在该时刻设定的发生开始地址（4）确定为关键路径的发生开始地址（步骤 a7），关键路径的发生开始地址的探索处理结束。

再有，在即使将发生开始地址设定为最前面的地址（1）来进行工作试验在输出引脚 1 上也不呈现正常的输出数据的情况下，在关键路径的探索方面失败，探索处理结束（步骤 a10）。

在通过这样做结束了关键路径的发生开始地址的确定之后，进行发生区间的确定。图 6 是示出探索发生关键路径的区间的工作程序的图。首先，测试处理器 10 将指令送给时序产生器 20，将全部地址的工作周期设定为失效周期 T1（步骤 b1）。将全部工作周期设定为失效周期 T1 后，测试处理器 10 将关键路径的发生结束地址（以下，简单地称为「发生结束地址」）设定为前面已确定的发生开始地址（步骤 b2）、即将关键路径发生区间（以下，简单地称为「发生区间」）只限定于发生开始地址，将与该发生区间对应的地址的工作周期设定为通过周期 T2（步骤 b3）。然后，对于半导体装置 100 进行预定的工作试验（步骤 b4），判定在输出引脚 1 上呈现的输出数据是否是正常值（步骤 b5）。

图 7A～图 7C 是示出发生区间与为了对其进行确认而设定的各地址的工作周期的关系的图。如图 7A 中所示，在上述的步骤 b2 中将发生结束地址设定为发生开始地址（4）的情况下，只将作为发生区间的地址（4）的工作周期变更为通过周期 T2，进行工作试验。

以这种方式进行实施的工作试验的结果，在输出引脚 1 上呈现的输出数据是与预期一致的正常的数据的情况下，将在该时刻设定的发生区间确定为关键路径的发生区间（步骤 b6），关键路径的发生区间的探索处理结束。

此外，工作试验的结果，在输出引脚 1 上呈现的输出数据不正常的情况下，测试处理器 10 下一步判断在该时刻设定的发生结束地址是否是测试周期的失效地址（7）（步骤 b7）。由于最初在上述的步骤 b2 中将发生开始地址（4）设定为发生结束地址，故判断为否定，测试处理器 10 将发生结束地址向后进 1，设定为地址（5）（步骤 b8），重复上述的步骤 b3 的工作周期的设定以后的处理。

如图 7B 中所示，在将发生结束地址向后进 1、设定为地址（5）的情况下，将从发生开始地址（4）到发生结束地址（5）为止作为发生区间来设定，将这两个地址（4）、（5）的工作周期设定为通过周期 T2，实施工作试验。

此外，在即使将地址（4）和（5）的工作周期设定为通过周期 T2 来

实施工作试验在输出引脚 1 上也不呈现正常的输出数据的情况下，如图 7C 中所示，在再将发生结束地址进 1、设定为地址（6）并将发生区间定为地址（4）~（6）之后，重复上述的步骤 b3 的工作周期的设定以后的处理。

通过这样做，将发生结束地址逐一向后行进、将从发生开始地址到发生结束地址为止的发生区间中包含的各地址的工作周期设定为通过周期 T2，通过每次都进行工作试验，重复该程序直到在输出引脚 1 上呈现正常的输出数据为止。例如，如图 7C 中所示，在将发生结束地址设定为地址（6）并将作为发生区间的地址（4）~（6）的各工作周期设定为通过周期 T2 来实施工作试验时在输出引脚 1 上呈现正常的输出数据的情况下，如上述那样，在步骤 b5（输出数据是否是正常的判定处理）中判断为肯定，将在该时刻的发生区间确定为关键路径的发生区间（步骤 b6），关键路径的发生区间的探索处理结束。

再有，在即使将发生结束地址设定为测试周期的失效地址（7）来进行工作试验在输出引脚 1 上也不呈现正常的输出数据的情况下，即、如果将发生结束地址设定为测试周期的失效地址（7），则由于再现图 5D 中示出的状态，故必定应该在输出引脚 1 上呈现正常的输出数据，但关于不呈现正常的输出数据这一点，由于存在按照在图 4 中示出的一系列的工作程序进行的关键路径的最前面的地址的探索工作中有错误这样的可能性，故此时在关键路径的探索方面失败，探索处理结束（步骤 b9）。

按照本实施例的半导体试验装置，使将预定的试验数据输入到半导体装置 100 中到能得到与其对应的输出数据为止的各工作时钟与各地址相对应，在最初将全部地址的工作周期设定为作为失效和通过的边界的失效周期 T1 之后，按顺序将输出引脚 1 附近的地址的工作周期变更为通过周期 T2，检验在将工作周期变更为通过周期 T2 时到哪个地址为止输出数据成为正常值，通过进行工作周期的部分变更和此时的输出数据的正确与否的判定，能探索关键路径的发生开始地址。

此外，在检测出了关键路径的发生开始地址之后，固定该开始地址，由该地址开始按顺序挪到处于后面的发生结束地址、使发生区间加长，检验在加长发生区间时到哪个地址为止输出数据成为正常值，通过进行工作周期的部分变更和此时的输出数据的正确与否的判定，能探索关键路径的发生范围。这样，如果知道关键路径的发生开始地址和发生区间，

则由于能通过对照设计数据等来确定成为实际的半导体装置 100 内的不良原因的相当部位，故改善高速工作时的传播延迟时间等的对策成为可能.

这样，使用本实施例的半导体试验装置，通过使实际的半导体装置 100 工作来进行关键路径的探索，与利用模拟来探索关键路径的情况相比，可大幅度降低编制探索程序的时间，而且可在接近于实际使用的状态下再现负载的设定等. 此外，由于实际上使半导体装置 100 工作来进行关键路径的探索，故与用模拟来再现各个构成要素的工作的情况相比，可大幅度缩短在探索方面所需要的时间.

再者，在成为关键路径的探索对象的半导体装置 100 中，也有下述的半导体装置，该半导体装置在内部具有 PLL 电路，与从外部输入的时钟信号（以下，称为「外部时钟」）同步地利用内部的 PLL 电路生成修正了占空比的时钟信号（以下，称为「内部时钟」），并与该已生成的内部时钟同步地工作. 迄今，对于这样的半导体装置 100，一般认为，如图 8 中所示，如果使外部时钟的周期较大地变动，则由 PLL 电路生成的内部时钟的周期大幅度地变乱，故不能保障半导体装置 100 的正常工作，难以使用实际的半导体装置 100 来探索关键路径.

但是，在上述的本实施例的半导体试验装置中，在图 4 中示出的步骤 a1 中，也可检验失效和通过的边界、使用其附近的稍许不同的工作周期 T1 和 T2 来进行关键路径的探索。因而，即使是将各地址的工作周期部分地从周期 T1 变更为周期 T2 的情况，也可减少对由半导体装置 100 内部的 PLL 电路生成的内部时钟的影响，使半导体装置 100 正常地工作，按照图 4 和图 6 中示出的一系列的程序进行关键路径的探索.

图 9 是示出部分地将半导体装置 100 的外部时钟设定为通过工作周期 T2 时的外部时钟与内部时钟的关系的图. 例如，如果只将地址（4）的工作周期变更为 T2，则虽然由半导体装置 100 中内置的 PLL 电路也将内部时钟的工作周期变更为 T2，但在其之后即使使外部时钟的工作周期回到周期 T1，内部时钟在受到几个地址的影响之后也收敛到周期 T1.

例如，在将全部测试周期的工作周期设定为 21nsec 时能得到的输出数据是不正常的失效状态、将工作周期设定为 22nsec 时能得到的输出数据是正常的通过状态、将工作周期设定为在其间的 21.5nsec 时能得到的输出数据是失效状态和通过状态交替地呈现的不稳定状态的情况

下，分别将失效工作周期设定为 21nsec、将通过工作周期设定为 22nsec。在这种情况下，由于这些周期的差是 22－21＝1nsec，是周期的约 5％，故不会使 PLL 电路的修正受到大的影响。

这样，虽然不能如图 2A 和图 2B 中所示那样只将打算检验的地址的工作周期设定为通过周期 T2，将除此以外的地址的工作周期正确地设定为通过周期 T1，但能将包含特定的地址的预定范围的工作周期设定为 T2 或与其近似的值。因而，按照图 4 和图 6 中示出的一系列的程序，即使对内置了 PLL 电路的半导体装置 100 也能大致正确地确定关键路径的发生开始地址和发生区间，能使实际的半导体装置 100 工作来进行关键路径的探索。

再有，本发明不限于上述实施例，在本发明的要点的范围内可实施各种变形。例如，在上述的实施例中，如图 5A－图 5D 中所示，将发生开始地址从最后面的地址开始按顺序逐一向前挪来探索关键路径的发生开始地址，但也可以 2 个以上的地址为单位来挪并检验此时的在输出引脚 1 上呈现的输出数据（对应于将 n-i 的 i 值设定为 2 以上的情况）。

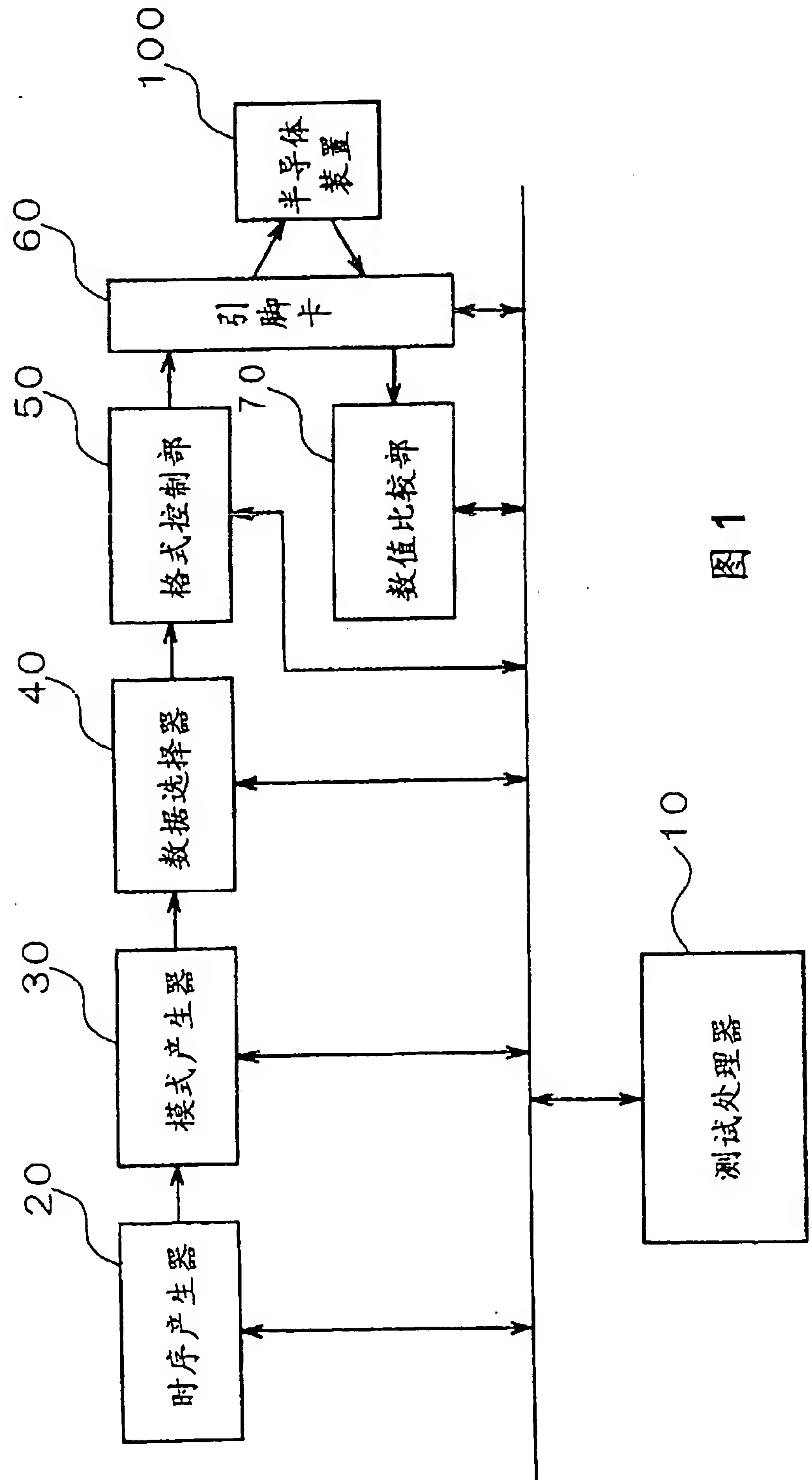
或者，使用 2 分探索法，首先，在最初将后半的全部工作周期变更为通过周期 T2，检验此时的输出数据，判定发生开始地址存在于前半部分还是存在于后半部分，其后将包含发生开始地址的范围 2 等分，将后半部分的地址的工作周期设定为通过周期 T2，检验输出数据。通过这样做，也可逐渐将包含发生开始地址的范围变窄，最终确定 1 个地址。在半导体装置 100 的电路规模大的情况下、即关键路径的发生地址存在于远离失效地址的部位的情况下，如果从测试周期的最终地址开始逐一回溯来检验，则要花费相当多的时间，但如果使用该方法，就可缩短在探索方面所需要的时间。

此外，在上述的实施例中，使用实施半导体装置 100 的各种功能试验的半导体试验装置来进行半导体装置 100 的关键路径的探索，但只要是能任意地设定时钟周期的装置，则也可不必使用很普通的半导体试验装置、而是使用其它的硬件来实现。

此外，在上述的实施例中，通过利用测试处理器 10 执行图 4 和图 6 中示出的工作程序来确定关键路径的发生开始地址和发生区间，但也可利用逻辑电路等硬件来实现测试处理器 10 执行的一系列的程序，只用硬件来实现在关键路径的探索方面必须的全部处理。

此外，在上述的实施例中，在确定关键路径的发生区间时，逐点地检测发生区间的发生开始地址和发生结束地址来进行区间的确定，但由于也有隔开 2 个部位以上发生关键路径的情况，故也可个别地探索这些多个部位的关键路径．例如，按照图 6 中示出的工作程序，确定关键路径的发生区间．在图 7C 的情况下，关键路径的发生区间存在于地址(4)~(6)．此时，真正发生关键路径的地址是地址（4）和（6）的 2 个部位．地址（5）与此无关．此时，将图 6 的算法反过来应用，将作为关键路径的发生区间的地址的通过工作周期 T2 区间替换为失效周期 T1，通过观察半导体装置的输出数据是否正常工作能够探索与关键路径的发生无关的地址．由此，结果可确定由多个部位的原因引起的关键路径的发生区间。

说　明　书　附　图



100
半导体装置
60
引脚卡
50
格式控制部
70
数值比较部
40
数据选择器
30
模式产生器
20
时序产生器
10
测试处理器

图 1

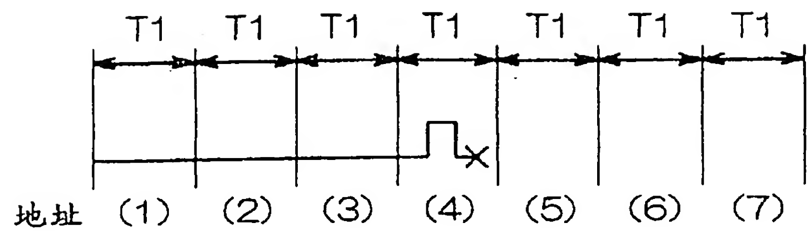


图 2A

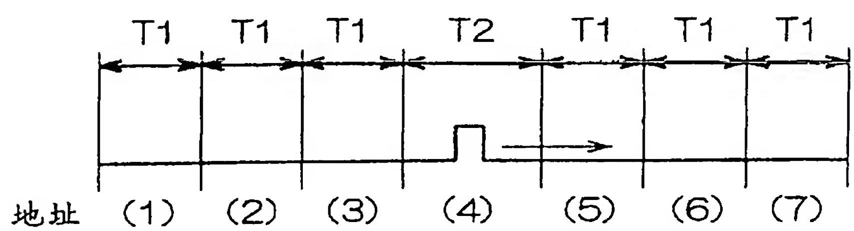
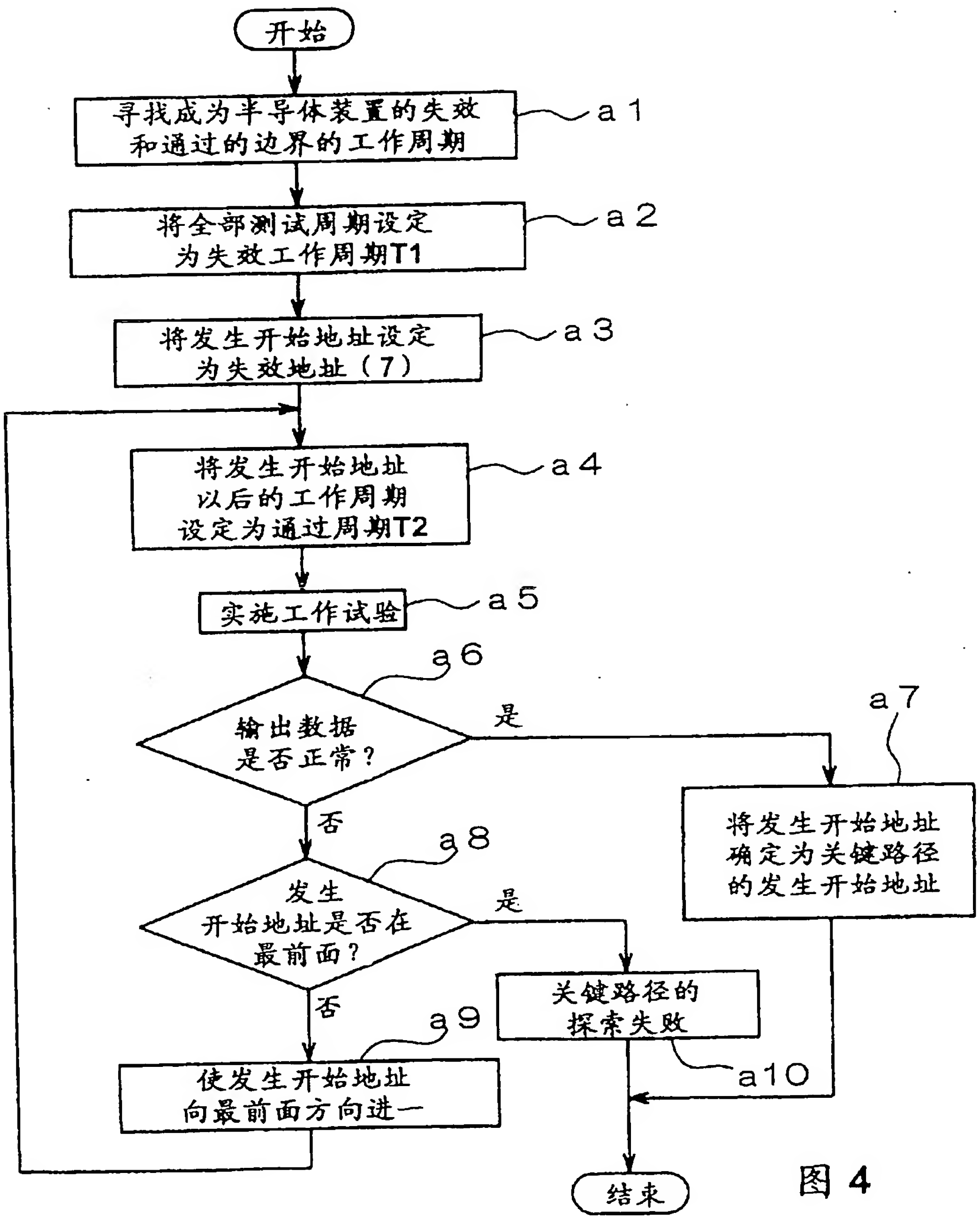


图 2B

地址	(1)	(2)	(3)	(4)	(5)	(6)	(7)
工作周期	t1	t2	t3	t4	t5	t6	t7
输入引脚1	0	1	0	1	0	1	0
输出引脚1	×	×	×	×	×	×	LorH

图3

99.01.15



开始
寻找成为半导体装置的失效和通过的边界的工作周期
a1
将全部测试周期设定为失效工作周期T1
a2
将发生开始地址设定为失效地址（7）
a3
将发生开始地址以后的工作周期设定为通过周期T2
a4
实施工作试验
a5
a6
输出数据是否正常？
是
a7
将发生开始地址确定为关键路径的发生开始地址
否
a8
发生开始地址是否在最前面？
是
关键路径的探索失败
a10
否
a9
使发生开始地址向最前面方向进一
结束

图 4

地址	(1)	(2)	(3)	(4)	(5)	(6)	(7)
发生开始地址							○
工作周期	T1	T1	T1	T1	T1	T1	T2

图 5A

地址	(1)	(2)	(3)	(4)	(5)	(6)	(7)
发生开始地址						○	
工作周期	T1	T1	T1	T1	T1	T2	T2

图 5B

地址	(1)	(2)	(3)	(4)	(5)	(6)	(7)
发生开始地址					○		
工作周期	T1	T1	T1	T1	T2	T2	T2

图 5C

地址	(1)	(2)	(3)	(4)	(5)	(6)	(7)
发生开始地址				○			
工作周期	T1	T1	T1	T2	T2	T2	T2

图5D

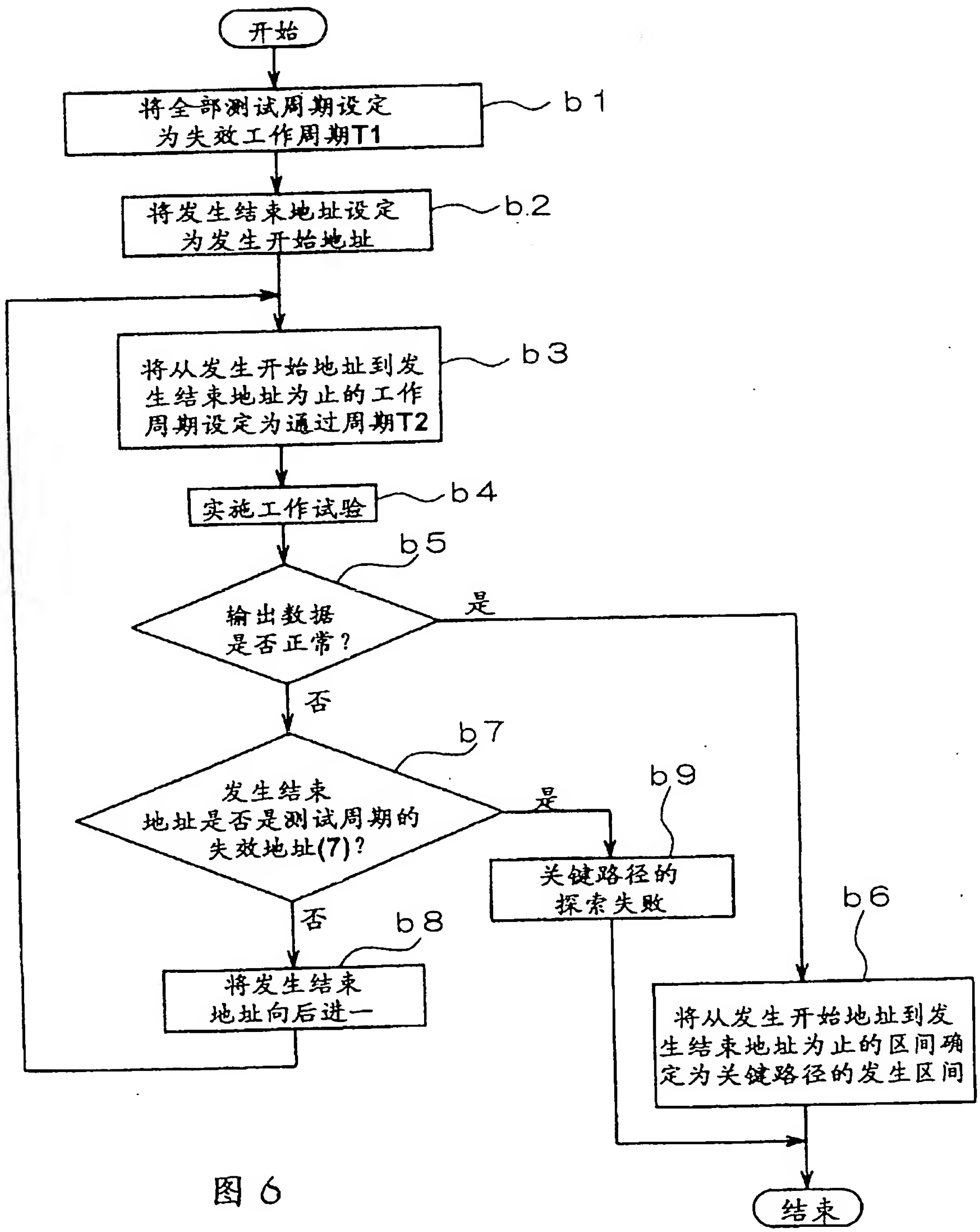
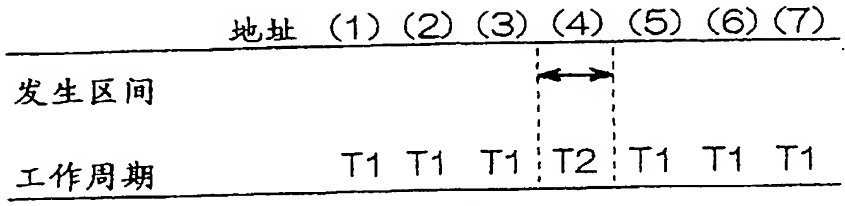
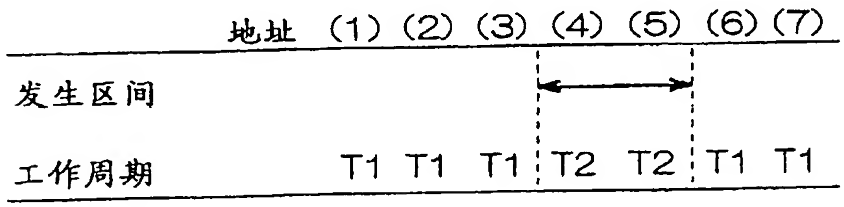

开始
将全部测试周期设定为失效工作周期T1
b1
将发生结束地址设定为发生开始地址
b2
将从发生开始地址到发生结束地址为止的工作周期设定为通过周期T2
b3
实施工作试验
b4
b5
输出数据是否正常？
是
否
b7
发生结束地址是否是测试周期的失效地址(7)？
是
b9
关键路径的探索失败
否
b8
将发生结束地址向后进一
b6
将从发生开始地址到发生结束地址为止的区间确定为关键路径的发生区间
结束

图 6



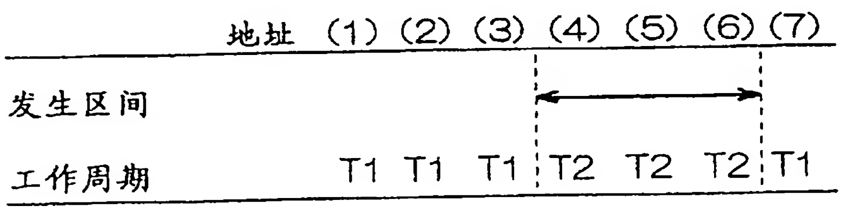
地址 (1) (2) (3) (4) (5) (6) (7)
发生区间
工作周期 T1 T1 T1 T2 T1 T1 T1

图 7A



地址 (1) (2) (3) (4) (5) (6) (7)
发生区间
工作周期 T1 T1 T1 T2 T2 T1 T1

图 7B



地址 (1) (2) (3) (4) (5) (6) (7)
发生区间
工作周期 T1 T1 T1 T2 T2 T2 T1

图 7C

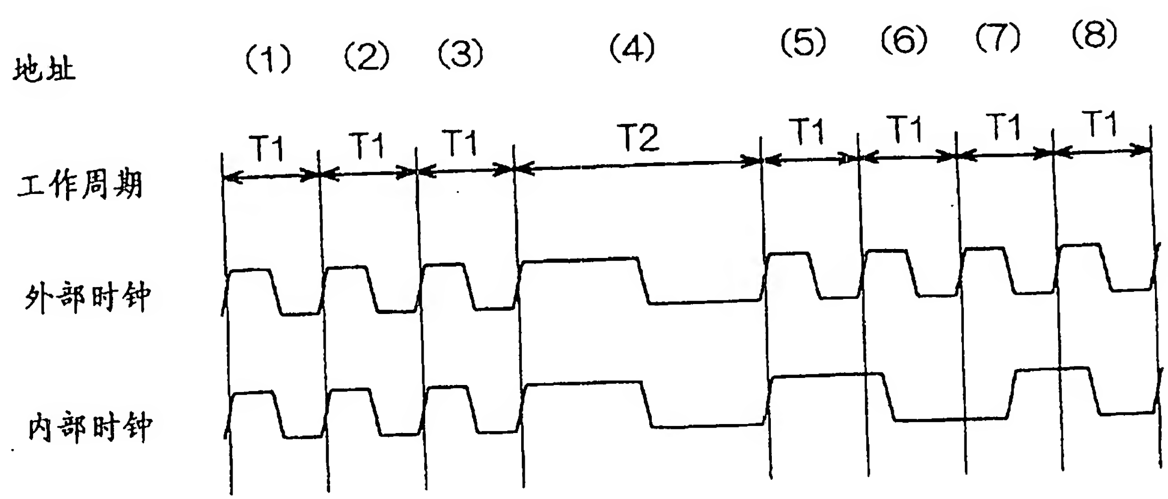


图 8

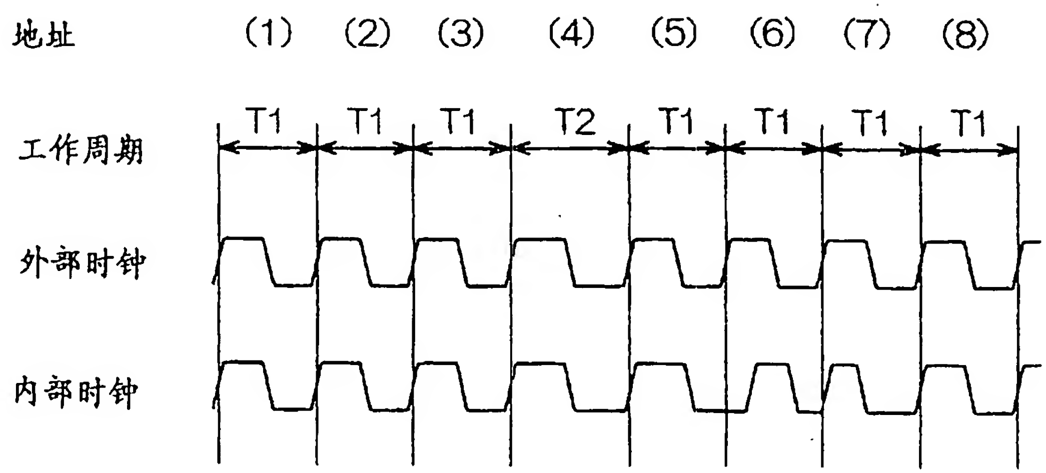


图 9

Key path searching method and system

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This invention discloses a method and system to search for a critical path which allows a quick and reliable search for a critical path by using an actual semiconductor device. When the number of the operating clock pulses between the input of a predetermined data to a semiconductor device and the output of the corresponding data is n pulses, each period of the n pulses is changed from a failing period T1 to a passing period T2 in order to search for a critical path.

Key path searching method and system

Description of corresponding document: US6829573

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a method and system to search for a critical path to identify critical paths in various large scale integrated circuits (LSI). In this specification, a "semiconductor device" means a logic circuit, memory circuit and analog circuit, or a whole semiconductor device composed of any combination thereof.

[0003] Today, the number of transistors integrated into LSI's has dramatically increased. Particularly, the circuits of logic LSI's including microprocessors as a typical device, memories, analog LSI's and system LSI's have been becoming increasingly complicated. In order to perform failure analyses on these large scale, complicated and further high speed LSI and to feed-back the results to device design, efforts to search out critical paths in the LSI's have been frequently made. The critical path means particular paths limiting the operating speed of the whole circuit in a signal propagation path in an LSI. For the design of an LSI, it is important to control the propagation time of these paths below predetermined values.

[0004] Hitherto, searches for a critical path in an LSI has been performed by using simulations based on the design data of an LSI. For each of circuits constituting an LSI, the simulation technology can calculate from the design data the propagation time to pass through various arithmetic circuits, memories and others from an input of a signal to the output. Therefore, when a predetermined test vector (a test pattern) is inputted, a calculation can obtain how it operates in the inside of the LSI and thus allows a search for a critical path.

[0005] On the other hand, the previous technique to obtain a critical path in an LSI by using simulation technology as described above has the following problems.

[0006] (1) It takes too much time to make a program which performs a simulation for finding out the critical paths for all logic signals.

[0007] (2) Because it does not operate actual circuits (semiconductor devices), it takes too much time to set a load and others that are impossible or difficult for simulations to represent.

[0008] (3) Because it performs the processing of massive amount of numerical data, it takes very much time for a search.

SUMMARY OF THE INVENTION

[0009] The present invention has been created in view of these problems. The object of the invention is to provide a method and system to search for a critical path which allows a quick and reliable detection of a critical path by using an actual semiconductor device.

[0010] A preferred embodiment of the method and system to searching for a critical path in accordance with the present invention is based on the following. The period of operation clock pulses is decreased up to a period T1 on which the device can not operate normally. Then, the operating clock pulse corresponding to the position of a critical path is changed to a little longer period T2, so that the semiconductor device can be normally operated. In consideration of this point, it is examined which pulse of n operating clock pulses between the input of data and the output of

the data has been changed from T1 to T2 for normally operating the semiconductor device. Thereby, the search for a critical path is performed.

[0011] Specifically, an operating clock producing means sets the periods of the n operating clock pulses to T1 or T2, and an test data input means inputs data to the semiconductor device. The semiconductor device operates corresponding to the inputted data in synchronization with the n operating clock pulses and outputs data. An output data determining means determines whether the output data from the semiconductor device is wrong or correct. When this output data is correct, that is when the semiconductor device normally operates, a search control means decides that a critical path exists at the position of the operating clock pulse with the period T2 and performs search processing for a critical path.

[0012] In this way, the present invention performs the search for a critical path by actually operating a semiconductor device. Compared to the case of searching for a critical path by a simulation technique, the search according to the present invention allows fast and reliable detection of a critical path. Further, the search of the present invention can operate a semiconductor device with the setting of a load and others and so allows search processing in consideration of actual operating conditions.

[0013] Further, by using the search control means described above, each period of the operation clock pulses from the nth pulse to the (n-i)th pulse and a period of the other are set to T2 and to T1, respectively, and whether the semiconductor device operates normally or not is examined. The value of (n-i) on which the semiconductor device operates normally is identified as a critical path generation start position. This is a first target. Also, by using the search control means, a period of the operation clock pulses included in a predetermined range including the critical path generation start position as the leading position thereof and a period of the other are set to T2 to T1, respectively. Then, whether the semiconductor device operates normally or not is examined. The narrowest range in which the semiconductor device operates normally is identified as a critical path generation segment. This is a second target. In this way, the present invention identifies a critical path generation start position and critical path generation segment and thereby allows an accurate search for a critical path generation position. As a result, it becomes easy to take measures such as a design change.

[0014] Yet further, the present invention is suitable for the search for a critical path in a semiconductor device including a PLL circuit which produces another internal clock pulses in synchronization with operating clock pulses inputted from the outside. The search method for critical path in accordance with the present invention also can operate a semiconductor device on a period T1 and T2 of operating clock pulses that are placed in the vicinity of the boundary of whether the semiconductor device operates normally or not. So, when the periods of the operation clock pulses inputted from the outside are changed between T1 and T2, the internal clock pulses produced by the internal PLL circuit are easy to follow the operating clock pulses. Therefore, the search method of the present invention, which searches for a critical path by changing the periods of the operation clock pulses as described above, is readily applicable to such semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a block diagram of the constitution of the semiconductor testing system in accordance with an embodiment of the invention;

[0016] FIGS. 2A-2B illustrate the principle of the search for a critical path utilized in the semiconductor testing system in accordance with an embodiment of the

invention:
[0017] FIG. 3 illustrates the relation between input and output patterns to a semiconductor device and the period of the operation clock pulses;
[0018] FIG. 4 illustrates an operating procedure to searching for a critical path generation start address;
[0019] FIGS. 5A-5D illustrate the relation between a generation start address and the operating periods of each address set to ascertain the generation start address;
[0020] FIG. 6 illustrates an operating procedure for searching a critical path generation segment;
[0021] FIGS. 7A-7C illustrate the relation between a generation segment and the operating periods of each address set to ascertain the generation segment;
[0022] FIG. 8 illustrates the relation between external clock pulses inputted to a semiconductor device including a PLL circuit therein and internal clock pulses; and
[0023] FIG. 9 illustrates the relation between external clock pulses inputted to a semiconductor device including a PLL circuit therein and internal clock pulses.

DESCRIPTION OF THE PREFERED EMBODIMENT
[0024] The semiconductor device testing system in accordance with an embodiment of the present invention inputs a predetermined pattern data to a semiconductor device searched for a critical path. At the same time, it operates the semiconductor device by setting the period of the operation clock pulse in each test cycle to a vicinity value on the boundary between a pass (normal operation) and a failure (abnormal operation) to search for a critical path. A feature of the present invention is in such an operation. The details on the semiconductor testing system in accordance with the embodiment of the invention will be explained with reference to the drawings.
[0025] FIG. 1 is a block diagram of the semiconductor testing system according to the embodiment. The semiconductor testing system as shown in the FIG. 1 includes the following various sections to input and output various signals necessary for a search operation on a semiconductor device 100 searched for a critical path. That is, it includes a tester processor 10, timing generator 20, pattern generator 30, data selector 40, format control section 50, pin-card 60 and digital comparing section 70.
[0026] The tester processor 10 controls the whole operation of the semiconductor testing system for carrying out a predetermined program based on the operating system (OS) and searching for a critical path in a semiconductor device 100. The timing generator 20 sets a basic period required for the search operation and produces various timing edges included within the basic period set. The pattern generator 30 produces pattern data to be inputted to each of the terminals, including a clock terminal, of the semiconductor device 100. The data selector 40 relates the various pattern data outputted from the pattern generator 30 to each corresponding terminal of the semiconductor device 100 which receives the pattern data. The format control section 50 performs waveform control for the semiconductor device 100 based on the pattern data produced by the pattern generator 30 and selected by the data selector 40 and based on the timing edges produced by the timing generator 20.
[0027] The pin-card 60 is also intended to provide a physical interface to the semiconductor device 100. For example, the pin-card 60 includes a driver which supplies predetermined pattern waveforms to corresponding terminals of the semiconductor device 100 and a comparator which compares voltage waveforms appearing on each terminal with the predetermined levels of a low level voltage and high level voltage. The digital comparing section 70 compares the data of expected

value for each terminal selected by the data selector 40 to the output data of each terminal of the semiconductor device 100.

[0028] The timing generator 20 produces clock signals and other timing signals supplied to the semiconductor device 100. The pattern generator 30 produces various data inputted to the semiconductor device 100. Further, the semiconductor device 100 receives the input of predetermined test data and is operated during the test cycles of a predetermined number, and the digital comparing section 70 identifies whether the resulting data outputted from the semiconductor device 100 is normal or not.

[0029] The timing generator 20, the pattern generator 30 and data selector 40, the digital comparing sections 70 and the tester processor 10, described above, corresponds to an operating clock pulse producing means, a test data input means, an output data determining means and a search control means, respectively.

[0030] The semiconductor testing system in accordance with the embodiment comprises such a configuration as described above. Hereinafter, the detailed operation to searching for a critical path in the semiconductor device 100 using the semiconductor testing system will be explained.

[0031] FIGS. 2A and 2B are intended to illustrate the principle of the critical path search which is performed by the semiconductor testing system of the embodiment. Referring to FIGS. 2A and 2B, addresses (1), (2) and so on correspond to the test cycle counts, that is the number of the operating clock pulses inputted. For example, the address (6) shows a position (circuit) which operates in synchronization with the sixth pulse from the input of a test pattern.

[0032] As shown in FIG. 2A, by gradually shortening the period of the operation clock pulse, the period causing a failed output pattern is referred to as T1. At this time, if it is possible to pinpoint an address corresponding to the circuit which does not operate normally and so cause the failed output pattern, the improper point is searched out as the point generating a critical path.

[0033] For example, FIG. 2A shows a case where an abnormal operation occurs at a position corresponding to the address (4) and the output pattern is failed. In this case, by changing the period of the fourth operation clock pulse corresponding to the address (4) to a period T2 a little longer than T1, a normal operation pattern can be obtained, as shown in FIG. 2B.

[0034] In this way, the operating periods of all the test cycles are set to the failing period T1. Then, it is examined which address corresponds to the operating period so increased as to result in a normal operation. Thus, an address generating a critical path can be searched out. The embodiment performs the search processing for a critical path by detecting both a critical path generation start address and a generation segment.

[0035] FIG. 3 shows the relation between the input and output patterns to the semiconductor device 100 and the periods of operation clock pulses. For example, it is assumed that, when seven operating clock pulses are inputted from the input of a predetermined test data (in FIG. 3, the data to the address (1) is "0") to an input pin 1 of the semiconductor device 100, an output data corresponding to the test data appears on the output pin 1. Thus, by checking whether the output data at the seventh pulse agrees with the expected value or not, it can be known whether the circuit operation corresponding to the address to be examined is normal or not.

[0036] For example, when all the operating periods of the addresses are T1 except for the address (4) with the period T2 as shown in FIG. 2B, each of the operating periods t1-t3 and t5-t7 is set to T1 and the period t4 is exclusively set to T2 as shown in FIG. 3. Only the period of the fourth operation clock pulse is set to T2 in

this way, and then the semiconductor device 100 is operated 7 clocks. After the operation, whether the output data appearing on the output pin 1 agrees with the expected value is checked.
[0037] Then, the search operation for a critical path will be divided into a search operation for a critical path generation start address and that for a critical path generation segment in the following explanation. For example, as shown in FIG. 3, it is assumed that, at the operations on 7 clock pulses from the input of test data to the input pin 1, the corresponding data is outputted to the output pin 1. Further, critical paths are assumed to exist at the positions corresponding to the addresses (4)-(6) in the following explanation.
[0038] FIG. 4 shows an operating procedure of the search for a critical path generation start address. At first, the tester processor 10 varies the periods of operation clock pulses supplied to the semiconductor device 100 so as to search for an operating period of the boundary between the operation of a pass and the operation of a failure (step a1). The variation of the operating periods is performed by sending an instruction to the timing generator 20. The operating periods corresponding to all the addresses are set to certain respective values and the output data on the output pin 1 obtained in synchronization with the seventh clock pulse is examined as shown in FIG. 3. Thus, it is determined whether the semiconductor device 100 operates normally on each operating clock pulse of the varied periods or not. In this way, the period T1 of a operation clock causing a failure and the period T2 of a operation clock resulting in a pass are determined on the boundary described above.
[0039] Next, tester processor 10 sends an instruction to the timing generator 20 to set the operating periods of all the addresses to the failing period T1 (step a2). All of the operating periods t1-t7 as shown in FIG. 3 are set to T1.
[0040] In this way, all the operating periods are set to the failing period T1. After that, the tester processor 10 sets a critical path generation start address (hereinafter, called simply as "a generation start address") to the address (7) at which the semiconductor device 100 fails (hereinafter, called simply as "a fail address") (step a3). The operating periods of the generation start address and each address later than it are set to the passing T2 (step a4). Then, a predetermined operating test is carried out on the semiconductor device 100 (step a5), and it is determined (step a6) whether the output data appearing on the output pin 1 is normal or not.
[0041] FIGS. 5A-5D show the relation between a generation start address and the operating period of each address set to ascertain the generation start address. FIG. 5A shows a case in which the generation start address is set to the address (7) in the step a3 described above. For this case, only the operating period of the nth operation clock pulse corresponding to the address (7) (in the embodiment n=7, so the seventh address) of n operation clock pulses is changed to T2 and the operating test is performed.
[0042] As a result of the operating test performed in this way, when the output data appearing on the output pin 1 is normal as expected, the generation start address set at that moment is determined as a critical path generation start address (step a7). The search process for a critical path generation start address is completed.
[0043] Further, as a result of the operating test, when the output data appearing on the output pin 1 is not normal, then the tester processor 10 determines whether the generation start address at that moment is the leading address (1) (step a8). At first, because the generating start address has been set to the fail address (7) in the step a3 described above, a negative decision is produced. Then, the tester processor 10 advances the generation start address toward the leading direction by one address to

set it to the address (6) (step a9). After that, the processing of the step a4 for setting an operating period and later steps are repeated.

[0044] As shown in FIG. 5B, when the generation start address is advanced by one and set to the address (6), the address (6) and later addresses, that is the addresses (6) and (7), are set to the passing period T2. Then, the operating test is carried out.

[0045] Further, an operating test is performed with the operating periods of the address (6) and (7) set to the passing period T2. When normal output data does not appear on the output pin 1 even in this test, the generation start address is further advanced to the address (5) as shown in FIG. 5C. Then, the processing of the step a4 for setting an operating period or later steps are repeated.

[0046] In these ways, the generation start address is advanced toward the leading side one by one, the operating periods of the generation start address and each of the later addresses are set to the passing period T2 and the operating test is carried out each time. This procedure is repeated until normal output data appears on the output pin 1. For example, as shown in FIG. 5D, the generation start address is set to the address (4) and the operating periods of the addresses (4)-(7) are set to the passing period T2, and then the operating test is performed. When normal output data appears on the output pin 1, the step a6 (to determine whether the output data is normal or not) as described above produces a positive decision, and the generation start address (4) at that time is determined as a critical path generation start address (step a7). The processing of search for a critical path is completed.

[0047] However, when normal output data does not appear on the output pin 1 even in the operating test in which the generation start address is set to the leading address (1), the search process is assumed to have failed in finding a critical path and is terminated (step a10).

[0048] After the identification of a critical path generation start address is finished in this way, the identification of a generation segment will be performed. FIG. 6 shows an operating procedure of the search for a critical path generation segment. At first, the tester processor 10 sends an instruction to the timing generator 20 to set the operating periods of all the addresses to the failing period T1 (step b1). After setting all the operating periods to the failing period T1, the tester processor 10 sets a critical path generation end address (hereinafter, called simply as "a generation end address") to the generation start address identified earlier (step b2). That is, the critical generation segment (hereinafter, called simply as "a generation segment") is limited only to the generation start address and the operating period of the address corresponding to this generation segment is set to the passing period T2 (step b3). And, a predetermined test is carried out on the semiconductor device 100 (step b4) and whether the output data appearing on the output pin 1 is a normal value or not is determined (step b5).

[0049] FIGS. 7A-7C each show the relation between a generation segment and the operating period of each address set for ascertaining the generating segment. When the generation end address is set to the generation start address(4) in the step b2 described above, the operating period of the address (4) only as a generation segment is changed to a passing period T2, as shown in FIG. 7A. Then, an operating test is carried out.

[0050] As a result of the operating test performed in this way, in the case where the output data appearing on the output pin 1 is normal as expected, the generation segment set at that time is identified as a critical path generation segment (step a6). Then, the processing of the search for a critical pass generation segment is completed.

[0051] Further, as a result of the operating test, when the output data appearing on

the output pin 1 is not normal, then the tester processor 10 determines whether the generation end address is the fail address (7) in the test cycle (step b7). At first, because only the generation start address (4) is set to the generation end address in the step b2 described above, a negative decision is produced. The tester processor 10 advances the generation end address backward by one address and sets it to the address (5) (step b8) and repeats the processing of the step b3 for setting a operating period described above and the later steps.

[0052] As shown in FIG. 7B, when the generation end address is advanced backward by one to the address (5), a segment from the generation start address (4) to the generation end address (5) is set as a generation segment. The operating periods of these two addresses (4), (5) are set to the passing period T2 and the operating test is performed.

[0053] When normal output data does not appear on the output pin 1 even in the operating test performed with the operating periods of the addresses (4), (5) set to the passing period T2, the generation end address is further advanced by one to the address (6) as shown in FIG. 7C. Thus, the generation segment includes the addresses (4)-(6) and then the processing of the step b3 described above for setting a operating period and the later steps are repeated.

[0054] In this way, the generation end address is advanced backward one by one and the operating period of each address included in the range from the generation start address to the generation end address is set to an passing period T2 and the operating test is carried out each time. This procedure is repeated until normal data appears on the output pin 1. For example, as shown in FIG. 7C, the generation end address is set to the address (6) and each operating period of the addresses from (4) to (6) as a generation segment is set to the passing period T2 and the operating test is carried out. Then, when normal output data appears on the output pin 1, a positive decision is produced in the step b5 (determining whether the output is normal or not) described above. The generation segment at that time is determined as a critical path generation segment (step b6) and the processing of the search for a critical path generation segment is completed.

[0055] On the other hand, when normal output data does not appear on the output pin 1 even in the operating test performed with the generation end address set to the fail address (7) in the test cycle, the search processing is assumed to have failed in finding a critical path. Then the search is terminated (step b9). Because, the condition in which the generation end address is set to the fail address (7) in the test cycle replicates the condition shown in FIG. 5D and so normal output data should appear on the output pin 1. Therefore, when normal output data does not appear, there is a possibility of errors in searching for the leading address of a critical path, which has been carried out according to a series of operating procedures shown in FIG. 4.

[0056] In the semiconductor testing system in accordance with the embodiment, each operating clock pulse corresponds to each of the addresses from the input of a predetermined test data to the semiconductor 100 until the corresponding output data is outputted. At first, the operating periods of all the addresses are set to a failing period T1 that is on the boundary between a failure and a pass. Then, the operating periods of the addresses in the vicinity of addresses outputting the resulting data to an output pin 1 are changed to a passing period T2 one by one. It is examined which address corresponds to the operating period changed to the passing period T2 before the output data becomes normal data. Thus, by performing both the partial change of the operating periods and the fail/pass identification of the data outputted in response to this change, a critical path generation start address can

be searched.

[0057] Further, after the detection of a critical path generation start address, the start address is fixed, a generation end address behind the start address is shifted one by one and so the generation segment is extended. Thus, the addresses included in the segment extended before the output data is changed to a normal value are examined. Therefore, by performing the partial change of the operating periods and the fail/pass identification of the data outputted in response to this change, a critical path generation range can be searched. When a critical path generation address and a generation segment are searched out in this way, by checking them against design data and others, the position of sources for failed operation in the semiconductor device 100 can be identified. Thus, it is possible to take measures such as a reduction of propagation delay time in high-speed operation.

[0058] In this way, by using the semiconductor testing system in accordance with the embodiment, the search for a critical path is performed based on the operation of the actual semiconductor device 100. In comparison with a search method for a critical path using simulations, the equipment can eliminate a substantial amount of time and effort to make a search program and can reproduce the setting of loads and others in condition close to an actual use of the semiconductor device. Further, because the search for a critical path is performed based on the operation of the actual semiconductor device 100, compared to the case of reproducing each operation of the elements constituting the device by simulations, the equipment can substantially reduce time required for a search.

[0059] On the other hand, some of the semiconductor devices 100 searched for a critical path include a PLL Circuit internally. They produce a clock signal (hereinafter, called as an internal clock) with a duty ratio corrected by the internal PLL circuit in synchronization with a clock signal (hereinafter, called as an external clock) inputted from the outside and operate in synchronization with the internal clock produced. Hitherto, for these semiconductor devices 100, a search for a critical path by using an actual semiconductor device 100 has been thought to be impossible. Because, as shown in FIG. 8, a large variation of the external clock significantly disturbs the period of the internal clock produced by the PLL circuit and so a normal operation of the semiconductor device 100 can not be guaranteed.

[0060] However, it is also possible that the semiconductor testing system in accordance with the embodiment described above, in the step a1 as shown in FIG. 4, determines the fail/pass boundary and performs the search for a critical path by using a little different operating periods T1 and T2 in close proximity of the boundary obtained. Therefore, when the operating period of each address partially is changed from T1 to T2, the internal clock produced by a PLL circuit in the semiconductor device 100 is little affected. Thus, the search for a critical path can be carried out with the normal operation of the semiconductor device 100 according to a series of the procedures shown in FIG. 4 and FIG. 6.

[0061] FIG. 9shows the relation between the external clock pulses and the internal clock pulses in a case where the periods of the external clock pulses inputted to the semiconductor device 100 is partially changed to the passing operating period T2. For example, by changing the operating period of the address (4) only to T2, the operating period of the internal clock pulse is also changed to T2 by a PLL circuit embedded in the device 100. And, even if the operating period of the external clock pulses is reset to T1 immediately after, the period of the internal clock pulses remains effected over a few addresses and then is convergent to T1.

[0062] For example, for the setting of all the operating periods of test cycles to 21 nsec, the output data obtained is not normal, that is in a fail state. For the setting of

ail the operating period to 22 nsec, the output data obtained is normal, in a pass state. For the setting of an intermediate period of 21.5 nsec, the output data obtained is an unstable state with alternating fail and pass states. In such a case, the failing operating period and the passing operating period are set to 21 nsec and 22 nsec, respectively. Then, because the difference between these periods is 22-21=1 nsec, that is only about 5% of the periods, the internal clock is not significantly subject to the effect of correction by the PLL circuit.

[0063] As described above, it is difficult to set accurately only the operating period of an address to be checked to the passing period T2 and the other to the failing period T1 as shown in FIGS. 2A and 2B. However, it is possible to set the operating periods in a predetermined range including a specified address to T2 or a value close to T2. Therefore, according to a series of the procedures shown in FIGS. 4 and 6, even for a semiconductor device 100 with a built-in PLL circuit, it is possible to accurately identify a critical path generation start address and a generation segment. Also, it is possible to search for a critical path in an actual semiconductor device 100 operating.

[0064] Now, the invention is not limited in the embodiments described above and various varied implementations are possible in the scope of the substance of the invention. For example, in the embodiment described above, as shown in FIGS. 5A-5D, the search for a critical path generation start address is performed by shifting the generation start address from the rearmost address toward the front address one by one. However, by shifting units of two or more addresses, the output data appearing on the output pin 1 may be also checked (corresponding to a case of i>=2 in the (n-i)).

[0065] Further, it is possible to use the binary search method. At first, all the operating periods of the addresses in the rear half are changed to the passing period T2 and the output data at this time is examined so as to determine whether a generation start address exists in the front half or in the rear half. Then, the range including the generation start address is divided into two portions, the operating periods of the addresses within the rear half portion are set to the passing period T2 and the output data is checked. In this way, a segment including a generation start address is gradually made narrower so that one address can be eventually identified. In cases where the semiconductor device 100 has a large-scale circuit and further a critical path generation address is far away from the fail address, it takes too much time to examine each address one by one from the end address in the test cycle. However, use of this method said above can reduce time required for the search.

[0066] Also, in the embodiments described above, a search for a critical path is carried out by using semiconductor testing system performing various function tests on the semiconductor device 100. However, as far as it is possible to arbitrarily set the period of clock pulses, the use of general-purpose semiconductor testing system is not necessary and other hardware may be used to realize an alternate.

[0067] Further, in the embodiments described above, the tester processor 10 carries out the operating procedures shown in FIG. 4 and FIG. 6 so as to identify a critical path generation start address and a generation segment. However, a series of the procedures performed by the tester processor 10 may be realized by using logic circuits and others, and thereby all the processing necessary for a search for a critical path may be realized only by hardware.

[0068] Still further, in the embodiments described above, on the identification of a critical path generation segment, a generation start address and a generation end address within the generation segment are identified one by one. However, critical paths may occur in two or more positions separated and so it is possible to

individually search for critical paths on these plural positions. For example, it is assumed that a critical path generation segment has been identified according to the procedures as shown in FIG. 6. In the case of FIG. 7C, a critical path generation segment exists in the addresses (4)-(6). Then, it is assumed that the two addresses (4), (6) really generate critical paths but the address (5) does not generate. In this case, an adverse application of the algorithm of FIG. 6 can be performed. The passing period T2 of the address segment included in the critical pass generation segment are replaced to the failing period T1. And then, by determining whether the output data of the semiconductor device is normal or not, it is possible to search out addresses having no connection to the occurrence of a critical path. Thereby, as a result, it is possible to identify a critical path generation segment caused by plural positions.

FIG. 1

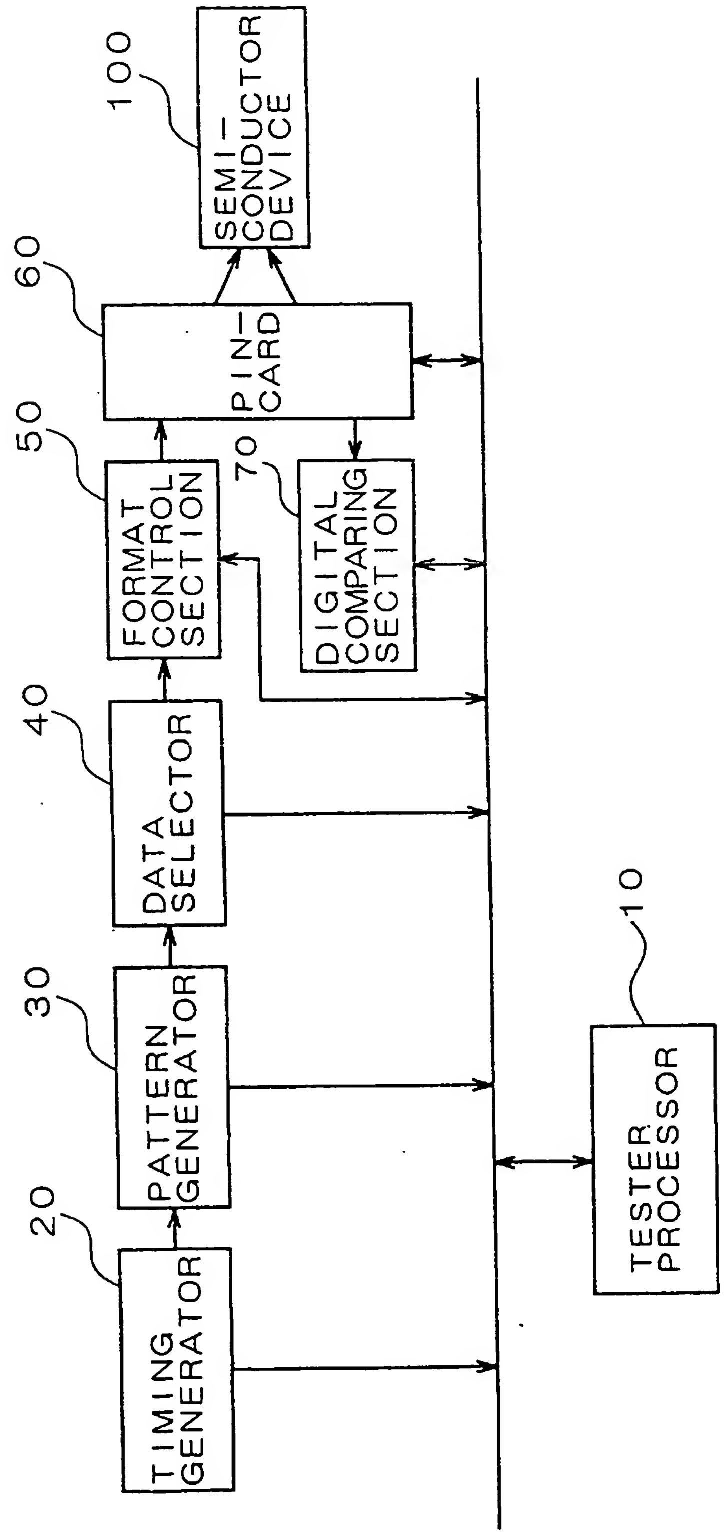
SEMI-CONDUCTOR DEVICE
100
PIN-CARD
60
FORMAT CONTROL SECTION
50
DIGITAL COMPARING SECTION
70
DATA SELECTOR
40
PATTERN GENERATOR
30
TIMING GENERATOR
20
TESTER PROCESSOR
10

FIG. 2A

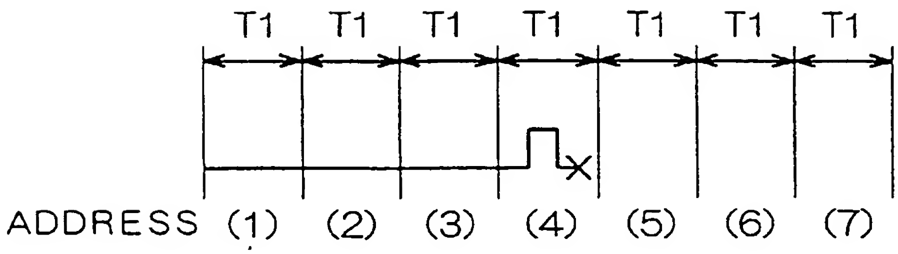

FIG. 2B

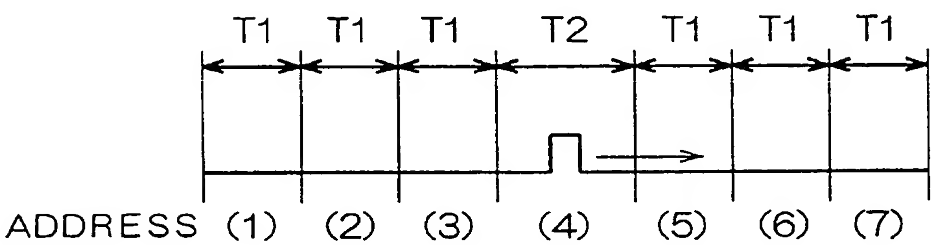

FIG. 3

ADDRESS	(1)	(2)	(3)	(4)	(5)	(6)	(7)
OPERATING PERIOD	t1	t2	t3	t4	t5	t6	t7
INPUT PIN 1	0	1	0	1	0	1	0
OUTPUT PIN 1	×	×	×	×	×	×	LorH